CLAIM

1. An arrangement for generating addresses for interleaving/de-interleaving sequences (x_1, x_2, x_3, ..., x_K) including a given number (K) of items, characterized in that it comprises at least one memory unit (22) having stored therein a plurality of records, each record being indicative of a respective set of interleaving/de-interleaving parameters (R, C, p, v) corresponding to at least one value of said given number (K) of items and generated by said at least one value.

2. The arrangement of claim 1, characterized in that, each value for said given number (K) of items identifying a corresponding set of parameters (R, C, p, v) for constructing a matrix (RxC) for arranging said sequences and affecting intra-row and inter-row permutation of said matrix to generate a permuted output matrix for generating said addresses, respective sets of said parameters (R, C, p, v) are available as records in said at least one memory unit (22) for all possible values of said given number of items (K).

3. The arrangement of claim 1 or claim 2, characterized in that, the value of said given number of items (K) being comprised in a given range of values, said at least one memory unit (22) has a number of said records stored therein that is substantially smaller than said given range of values.

4. The arrangement of claim 3, characterized in that each said record in said at least one memory unit (22) is identified by a respective pointer and associated with said at least one memory unit (22) is a pointer retrieval

circuit (20) configured for generating for each value of said given number of items (K) in said given range a corresponding pointer pointing to a respective record in said at least one memory unit (22).

5. The arrangement of claim 4, characterized in that said pointer retrieval circuit (20) comprises:

- a circuit (20a) sensitive to said given number of items (K) to derive therefrom a set of most significant bits of said pointers, and
- a respective memory unit (20b) having stored therein the remaining, least significant bits of said pointers.

6. The arrangement of claim 5, characterized in that said circuit (20a) comprises:

- a plurality of comparators (201, 202, 203) to compare said given number of items (K) with a number of given thresholds, and
- a logic unit (204) for combining the outcome of the comparisons carried out in said comparators (201, 202, 203) and derive therefrom said set of most significant bits of said pointers

7. The arrangement of claim 2, characterized in that said at least one memory unit (22) comprises, for each said record, at least one flag signal taking one of a first (0) and a second (1) logical value, said flag being set at said second logical value (1) when said given number of items (K) for the corresponding record is equal to the product of the number of rows (R) and the number of columns (C) in said matrix and said number of columns (C) in said matrix equals the value of the parameter (P) used for said intra-row permutation plus 1.

8. The arrangement of any of the previous claims, characterized in that it comprises arithmetic circuitry exempt from multipliers and dividers for generating a pseudo-random sequence of the type (a*b mode c) for producing a permutation pattern for use in said intra-row permutation.

9. The arrangement of any of the previous claims, characterized in that it comprises first and second permutation modules for performing said intra-row and said inter-row permutations, and in that said module for performing an inter-row permutation is arranged upstream of said module for performing intra-row permutation.

10. The arrangement of claim 9, characterized in that it comprises an intra-row module for producing a sequence (q) for performing said intra-row permutation, said intra-row module being configured for assigning $q_0 = 1$ to be the first prime integer in said sequence (q) and determining the prime integer q_i in the sequence to be a least prime integer such that the greatest common divisor $(q_i, p - 1) = 1$, $q_i > 6$, and $q_i > q_{(i-1)}$ for each $i = 1, 2, \ldots, R - 1$.

11. The arrangement of claim 10, characterized in that said intra-row module comprises:

- a prime numbers table for reading at least the prime integer therefrom, and
- a look up table for managing the greatest common divisor operation.

12. A method of generating addresses for interleaving/de-interleaving sequences $(x_1, x_2, x_3, \ldots, x_K)$

including a given number (K) of items, characterized in that it comprises the step of

- generating, on the basis of at least one value of said given number (K) of items, records indicative of a respective set of interleaving/de-interleaving parameters (R, C, p, v), and

- storing (22) in at least one memory unit said set of interleaving/de-interleaving parameters (R, C, p, v).

13. The method of claim 12, characterized in that, each value for said given number (K) of items identifying a corresponding set of parameters (R, C, p, v) for constructing a matrix (RxC) for arranging said sequences and affecting intra-row and inter-row permutation of said matrix to generate a permuted output matrix for generating said addresses, it comprises the step of making respective sets of said parameters (R, C, p, v) available as records in said at least one memory unit (22) for all possible values of said given number of items (K).

14. The method of claim 12 or claim 13, characterized in that, the value of said given number of items (K) being comprised in a given range of values, it comprises the step of storing in said at least one memory unit (22) a number of said records that is substantially smaller than said given range of values.

15. The method of claim 14, characterized in that it comprises the steps of identifying each said record in said at least one memory unit (22) by means a respective pointer and generating for each value of said given number of items (K) in said given range a corresponding pointer pointing to a respective record in said at least one memory unit (22).

16. The method of claim 15, characterized in that comprises the step of retrieving said pointers by:

- deriving from said given number of items (K) a set of most significant bits of said pointers, and
- storing the remaining, least significant bits of said pointers in a respective memory unit (20b).

17. The method of claim 16, characterized in that comprises the steps of:

- comparing (201, 202, 203) said given number of items (K) with a number of given thresholds, and
- combining (204) the results of said comparisons (201, 202, 203) to derive therefrom said set of most significant bits of said pointers

18. The method of claim 13, characterized in that it comprises the step of storing, for each said record, at least one flag signal taking one of a first (0) and a second (1) logical value, said flag being set at said second logical value (1) when said given number of items (K) for the corresponding record is equal to the product of the number of rows (R) and the number of columns (C) in said matrix and said number of columns (C) in said matrix equals the value of the parameter (P) used for said intra-row permutation plus 1.

19. The method of any of the previous claims 12 to 18, characterized in that it comprises the step of generating a pseudo-random sequence of the type (a*b mode c) for producing a permutation pattern for use in said intra-row permutation, said generating step being carried out by means of a linear algorithm exempt from multiplications and divisions.

20. The method of any of the previous claims 12 to 19, characterized in that said inter-row permutation is performed before said intra-row permutation.

21. The method of claim 20, characterized in that it comprises the step of producing a sequence (q) for performing said intra-row permutation, said intra-row module being configured for assigning $q_0 = 1$ to be the first prime integer in said sequence (q) and determining the prime integer q_i in the sequence to be a least prime integer such that the greatest common divisor $(q_i, p - 1) = 1$, $q_i > 6$, and $q_i > q_{(i-1)}$ for each $i = 1, 2, \ldots, R - 1$.

22. A turbo encoder including at least one of an interleaver and a de-interleaver module, said at least one module including an arrangement for generating addresses according to any of claims 1 to 11.

23. A turbo decoder including at least one of an interleaver and a de-interleaver module, said at least one module including an arrangement for generating addresses according to any of claims 1 to 11.

24. A computer program product directly loadable in the memory of a digital computer and including software code portion for performing the method of any of claims 12 to 21 when the product is run on a computer.